VLSID 2019 Preliminary Technical Program

***The nine best paper candidates are marked with* [BPC]**

Day 1 – January 7, 2019 (Monday)		
Track A	**Track B**	**Track C**
Registration		
Inauguration Ceremony		
Keynote 1		
Keynote 2		
Break		
Track 1A: Embedded Systems – I Session Chair: Prof. Aviral Shrivastava, Arizona State Univ.	**Track 1B: Analog/Mixed Signal – I** Session Chair: Prof. Mukul Sarkar, IIT Delhi	**Track 1C: Digital Design – I** Session Chair: Sourav Roy, NXP
[BPC] *Synthesizing Performance-aware (m,k)-firm Control Execution Patterns under Dropped Samples* Sumana Ghosh, Dey Soumyajit and Pallab Dasgupta	[BPC] *Ultra Low Energy Reduced Switching DAC for SAR ADC* Japesh Vohra and Vinayak Gopal Hande	[BPC] *Low-Complexity Continuous-Flow Memory-Based FFT Architectures for Real-Valued Signals* Jinti Hazarika, Mohd Tasleem Khan and Rafi Ahamed
[BPC] *Write Variation Aware Non-Volatile Buffers for On-Chip Interconnects* Khushboo Rani and Hemangee Kapoor	*Energy Efficient Bidirectional Equalized Transceiver with PVT Insensitive Active Termination* Antroy Roy Chowdhury, Nijwm Wary and Pradip Mandal	*Reducing the Overhead of Stochastic Number Generators Without Increasing Error* Yudai Sakamoto and Shigeru Yamashita
Performance Enhancement of Caches in TCMPs using Near Vicinity Prefetcher Dipika Deb, John Jose and Maurizio Palesi	*A Current Efficient Output Capacitor-Less LDO Regulator with Auto-Low Power Mode and Feed-forward Compensation* Abirmoya Santra and Qadeer Khan	*Low Complexity & Improved Efficiency of Encoded Data Using Peres Half Adder in BWA with Testable Feature* Tripti Nirmalkar, Deepti Kanoujia and Kshitiz Varma
EdgeCoolingMode: An Agent Based Thermal Management Mechanism for DVFS Enabled Heterogeneous MPSoCs Somdip Dey, Enrique Zaragoza Guajardo, Karunakar Reddy Basireddy, Xiaohang Wang, Amit Kumar Singh and Klaus McDonald-Maier	*MOS Varactor RO architectures in Near Threshold Regime using Forward Body Biasing techniques* Lalit Dani, Neeraj Mishra and Anand Bulusu	*A Systematic Approach for Acceleration of Matrix-Vector Operations in CGRA through Algorithm-Architecture Co-design* Farhad Merchant, Tarun Vatwani, Anupam Chattopadhyay, Somyendu Raha, S K Nandy, Ranjani Narayan and Rainer Leupers
LUNCH [1:00 – 2:00 pm]		
Keynote 3		
Panel		
Break		

Track 2A: Security – I Session Chair: Prof. Debdeep Mukhopadhyay, IIT Kharagpur	**Track 2B: Test and Validation – I** Session Chair: Prof. Masahiro Fujita, University of Tokyo	**Track 2C: RF Design** Session Chair: Prof. Tarun Bhattacharyya, IIT Kharagpur
[BPC] *A State Encoding Methodology for Side-Channel Security vs. Power Trade-off Exploration* Richa Agrawal, Mike Borowczak and Ranga Vemuri	**[BPC]** *A Binary Decision Diagram Approach to On-line Testing of Asynchronous Circuits* Pradip Biswal and Santosh Biswas	**[BPC]** *Analysis and Design of Low Phase Noise LC Oscillator for Sub-mW PLL-Free Biomedical Receivers* Abhishek Srivastava and Maryam Shojaei Baghini
An Efficient Memory Zeroization Technique Under Side-Channel Attacks Ankush Shrivastava and Prokash Ghosh	*RTL Test Generation on Multi-Core and Many-Core Architectures* Aravind Krishnan Varadarajan and Michael Hsiao	*A 19.3-24.8 GHz Dual-Slope VCO in 65-nm CMOS for Automotive Radar Applications* Vipul Jain, Saurabh Kumar Gupta, Vishal Khatri and Gaurab Banerjee
Two-Pattern Delta-IDDQ Test for Recycled IC Detection Prattay Chowdhury, Ujjwal Guin, Adit Singh and Vishwani Agrawal	*On-chip MISR compaction technique to reduce diagnostic effort and test time* Jaidev Shenoy, Virendra Singh, Kelly Ockunzzi and Kushal Kamal	*IIP3 Improvement in Subthreshold LNAs using Modified Derivative Superposition Technique for IoT Applications* Anant Rungta and Kavindra Kandpal
Parallelization of brute-force attack on MD5 hash algorithm in FPGA Maruthi Gillela, Vaclav Prenosil and Venkat Reddy Ginjala	*RSBST: A Rapid Software-based Self-test Methodology for Processor Testing* VM Suryasarman, Santosh Biswas and Aryabartta Sahu	*Enhanced IIP2 Chopper Stabilized Direct Conversion Mixer Architecture* Rohit Rothe and Rajesh Zele

Day 2 – January 8, 2019 (Tuesday)		
Track A	**Track B**	**Track C**
Registration		
Keynote 4		
Keynote 5		
Break		
Track 3A: Power and Energy – I Session Chair: Prof. Aryabartta Sahu, IIT Guwahati	**Track 3B: CMOS Devices** Session Chair: Prof. Sudeb Dasgupta, IIT Roorkee	**Track 3C: Emerging Tech – I** Session Chair: Prof. Rajat Pal, University of Calcutta
[BPC] *Power and Area Efficient Approximate Heterogeneous 8T SRAM for Multimedia Applications* Pramod Kumar Bharti, Neelam Surana and Joycee Mekie	**[BPC]** *An Unified Charge Centroid Model for Silicon and Low Effective Mass III-V Channel Double Gate MOS Transistors* Amratansh Gupta, Mohit	*Modelling and fabrication of mixing in low-cost passive PDMS micromixers* T Pravinraj and Rajendra Patrikar

	Ganeriwala and Nihar Mohapatra	
Ultra Low Power Digital Front-End for Single Lead ECG Acquisition Sanket Thakkar and Biswajit Mishra	*Optimization of Multiple Physical Phenomena through a Universal* Metric in Junctionless Transistors Manish Gupta and Abhinav Kranti	*Design of Continuous-Flow Lab-on-Chip with 3D Microfluidic Network for Sample Preparation* Tapalina Banerjee, Sudip Poddar, Sarmishtha Ghoshal and Bhargab Bhattacharya
Scheduling of Dual Supercapacitor for Longer Battery Lifetime in Systems with Power Gating Sumanta Pyne	*Delay Skew Reduction in IO Glitch Filter* Kiran Gopal and Avanish K	*Security Assessment of Microfluidic Fully-Programmable-Valve-Array Biochips* Mohammed Shayan, Sukanta Bhattacharjee, Yong-Ak Song, Krishnendu Chakrabarty and Ramesh Karri
An Energy Efficient In-Memory Computing Machine-Learning Classifier Scheme Shixiong Jiang, Sheena Priya, Naveena Elango, James Clay and Ramalingam Sridhar	*Insights on anisotropic dissipative quantum transport in n-type Phosphorene MOSFET* Madhuchhanda Brahma, Arnab Kabiraj and Santanu Mahapatra	*Improved Look-ahead Approaches for Nearest Neighbor Synthesis of 1D Quantum Circuits* Anirban Bhattacharjee, Chandan Bandyopadhyay, Robert Wille, Rolf Drechsler and Hafizur Rahaman
Break		
Track 4A: Intelligence on Silicon Session Chair: Dr. Manish Sharma, Samsung	**Track 4B: Design Automation** Session Chair: Prof. Susmita Sur-Kolay, ISI Kolkata	**Track 4C: Embedded Systems – II** Session Chair: Prof. Anshul Kumar, IIT Delhi
UniWiG: Unified Winograd-GEMM Architecture for Accelerating CNN on FPGAs Kala S, Jimson Mathew, Babita Jose and Nalesh S	*RiverOpt: A Multiobjective Optimization Framework based on Modified River Formation Dynamics Heuristic* Satyabrata Dash, Sukanta Dey, Anish J. Augustine, Rudra Sankar Dhar, Jan Pidanič, Zdeněk Němec and Prof. Gaurav Trivedi	*Criticality Aware Soft Error Mitigation in the Configuration Memory of SRAM based FPGA* Swagata Mandal, Sreetama Sarkar, Wong Ming Ming, Anupam Chattopadhyay and Amlan Chakrabarti
The Ramifications of Making Deep Neural Networks Compact Nandan Kumar Jha, Sparsh Mittal and Govardhan Mattela	*Structural and Behavioural Facets of Digital Microfluidic Biochips with Hexagonal-Electrode-based Array* Amartya Dutta, Riya Majumder, Debasis Dhal and Rajat Kumar Pal	*Multidimensional Grid Aware Address Prediction for GPGPU* Shivani Tripathy, Debiprasanna Sahoo and Manoranjan Satpathy
Machine Learning based Power Efficient Approximate 4:2 Compressors for Imprecise Multipliers Ravindra JVR and Lavanya Maddisetty	*Parasitic-Aware Automatic Analog CMOS Circuit Design Environment* Subhash Patel and Rajesh Thakker	*Efficient Heap Data Management on Software Managed Manycore Architectures* Jing Lu, Jinn-Pean Lin and Aviral Shrivastava
MAVI: Mobility Assistant for Visually	*Ultra Low Power Low Frequency*	*In situ Latency Monitoring for*

Impaired Using Deep Learning and Cloud Services Rajesh Kedia, Anupam Sobti, Mukund Rungta, Sarvesh Chandoliya, Akhil Soni, Anil Kumar Meena, Chrystle Myrna Lobo, Richa Verma, M. Balakrishnan and Chetan Arora	*On-Chip Oscillator for Elapsed Time Counter* Sachin Kalburgi, Deven Gupta, Sampath Holi, Rohit Shetty, Shripad Annigeri, Sujata Kotabagi, Shraddha Hiremath, Dr. Saroja Siddamal and Dr. Nalini Iyer	*Heterogeneous Real-time Systems* Martin Geier, Tobias Burghart, Martin Hackl and Samarjit Chakraborty
Lunch [1:00 – 2:00 pm]		
Keynote 6		
Panel		
Tea Break		
Track 4C: IoT and CPS Session Chair: Dr. Kaushik Saha, Samsung	**Track 5B: Analog/Mixed-Signal– II** Session Chair: Prof. Qadeer Khan, IIT Madras	**Track 5C: Digital Design – II** Session Chair: Prof. Anupam Chattopadhyay, NTU, Singapore
Investigation of Unified emerging-NVM SoC Architecture for IoT-WSN Applications Vivek Parmar, Swatilekha Majumdar, Preeti Ranjan Panda and Manan Suri	*A Mismatch Resilient 16-bit 20 MS/s Pipelined ADC* Satyajit Mohapatra, Dr. Hari Shanker Gupta, Nihar Mohapatra, Sanjeev Mehta, Arup Roy Chowdhury and Nisha Pandya	*High-Throughput and High-Speed Polar-Decoder VLSI-Architecture for 5G New Radio* Rahul Shrestha, Pooja Bansal and Srikant Srinivasan
A 75-µW 2.4 GHz Wake-up Receiver in 65-nm CMOS for Neonatal Healthcare Application Kundan Kumar, Raghunath K P, Akshay Muraleedharan, Javed S Gaggatur and Gaurab Banerjee	*Large dynamic range Readout Integrated Circuit for Infrared Detectors* Dr. Hari Shanker Gupta, Dinesh K Shrama, Maryam Shojaei Baghini, A S Kiran Kumar, Sanjeev mehta and Arup Roy Chowdhury	*VLSI Architectures for Jacobi Symbol Computation* Ayan Palchaudhuri and Anindya Sundar Dhar
Perturbation based Workload Augmentation for Comprehensive Functional Safety Analysis Prasanth V, Rubin Parekhji and Bharadwaj Amrutur	*Current DAC based -40dB PSRR Configurable Output LDO in BCD Technology* Vivek Tyagi, Vikas Rana, Laura CAPECCHI, Marcella CARISSIMI, Riccardo ZURLA and Marco Pasotti	*Soft Error Resilient and Energy Efficient Dual Modular TSPC Flip-Flop* Shubhanshu Gupta and Joycee Mekie
A Double Pumped Single-line-cache SRAM Architecture for Ultra-low Energy IoT and Machine Learning Applications Arijit Banerjee and Benton H. Calhoun	*Modeling and Characterization of VBUS Power Discharge for Embedded Superspeed USB Host/Devices* Maneesh Pandey, Mohit Goyal, Parul Kumar Sharma and Rohit Sharma	*k-core: Hardware Accelerator for k-mer Generation and Counting used in computational genomics* Simmi M Bose, Varsha S Lalapura, S Saravanan and Madhura Purnaprajna
Awards and Cultural Program		
Banquet Dinner		

Day 3 – January 9, 2019 (Wednesday)		
Track A	**Track B**	**Track C**
Registration		
Keynote 7		
Keynote 8		
Break		
Track 6A: Security – II Session Chair: TBD	**Track 6B: Test and Validation - II** Session Chair: TBD	**Track 6C: Emerging Tech – II** Session Chair: TBD
Novel Randomized & biased Placement For FPGA Based Robust Random Number Generator with Enhanced Uniqueness Arjun Chauhan, Vineet Sahula and Atanendu Mandal	*Improving Performance of Path Based Equivalence Checker using Counter-example* Ramanuj Chouksey, Chandan Karfa and Purandar Bhaduri	*An Efficient Design Approach for Implementation of 2 bit Ternary Flash ADC Using Optimized* Complementary TFET Devices Sanjay Vidhyadharan, Abhay SV, Ramakant ., A.Krishna Shyam, Mohit P Hirpara, Tanmay Chaudhary and Surya Shankar Dan
SoCINT: Resilient System-on-Chip via Dynamic Intrusion Detection Amr Sayed Ahmed, Jawad Haj-Yahya and Anupam Chattopadhyay	*Selective Sensitization of Useless Sneak-Paths for Test Optimization in Memristor-Arrays* Manobendra Nath Mondal, Susmita SurKolay and Bhargab Bhattacharya	*Novel Low and High Threshold TFET Based NTI and PTI Cells Benchmarked With Standard 45 nm CMOS Technology for Ternary Logic Applications* Ramakant ., Sanjay Vidhyadharan, A. Krishna Shyam, Mohit Hirpara, Tanmay Chaudhary and Surya Shankar Dan
Linear Approximation and Differential Attacks on Logic Locking Techniques Ghanshyam Bairwa, Souvik Mandal, Tatavarthy Venkat Nikhil and Bodhisatwa Mazumdar	*A Methodology for SAT-based Electrical Error Debugging during Post-silicon Validation* Binod Kumar, Masahiro Fujita and Virendra Singh	*A Capacity-Aware Wash Optimization for Contamination Removal in Programmable Microfluidic Biochip Devices* Piyali Datta, Arpan Chakraborty and Rajat Kumar Pal
Efficient Post-Silicon Validation of Network-on-Chip using Wireless Links Sidhartha Sankar Rout, Kanad Basu and Sujay Deb	*Test Configuration Generation for different FPGA Architectures for Application Independent Testing* Shukla Banik, Suchismita Roy and Bibhash Sen	*Optimizing Quantum Circuits for Modular Exponentiation* Rakesh Das, Anupam Chattopadhyay and Hafizur Rahaman
Break		
Track 7A: Embedded Systems - III Session Chair: Prof. Sharad Sinha, IIT Goa	**Track 7B: Digital Design – III** Session Chair: Prof. Hafizur Rahaman, IIEST, Shibpur	**Track 7C: Power and Energy - II** Session Chair: Arun Joseph, IBM
Write Variation aware Cache Partitioning for improved lifetime in Non-Volatile Caches	*Design and Physical Implementation of Array Signal Processor ASIC for Sector Imaging*	*Heterogeneity Aware Power Abstraction for Hierarchical Power Analysis*

Arijit Nath and Hemangee Kapoor	*Systems* Jayaraj Kidav, Dr. N M Sivamangai, Dr. Perumal M Pillai and Sreejeesh S G	Arun Joseph, Spandana Rachamalla, Shashidhar Reddy and Nagu Dhanwada
Applying Modified Householder Transform to Kalman Filter Farhad Merchant, Tarun Vatwani, Anupam Chattopadhyay, Somyendu Raha, S K Nandy, Ranjani Narayan and Rainer Leupers	*Low Power Design Technique in Passive Tag to Reduce the EMD Noise for Reliable Communication with Reader* Shankar Joshi, Rahul Pathak and Raghavendra Kongari	*HEART: A Heterogeneous Energy-Aware Real-Time scheduler* Sanjay Moulik, RAJESH DEVARAJ and Arnab Sarkar
Area efficient & High performance Word line Segmented architecture in 7nm FinFET SRAM compiler Vinay Kumar, Neeraj Kapoor, Sudhir Kumar, Monila Juneja and Amit Khanuja	*Allowing Switching off Periphery Voltage Island Instead of Doing it per Instance Through Periphery VDD Collapse in SRAMs* Krashna Nand Mishra, Ruchin Jain, Shailendra Sharad and Ravindra Shrivastava	*Adaptive Fractional Open Circuit Voltage Method for Maximum Power Point Tracking in a Photovoltaic Panel* Shubham Negi, Ashis Maity, mrigank sh and Amit Patra
Design of an optimized CMOS ELM accelerator Manoj Sharma, Umesh Lohani, Vivek Parmar and Manan Suri	*Majority Logic: Prime Implicants and n-input Majority Term Equivalence* Rajeswari Devadoss, Kolin Paul and M. Balakrishnan	*Energy Efficient Power Distribution on Many-Core SoC* Mustafa Shihab and Vishwani Agrawal
Lunch [1:00 – 2:00 pm]		
Keynote 9		
Panel		
Tea Break		
Interactive Presentation (IP) Poster Session [4:30 – 6:00 pm]		
Current Collapse reduction technique using N-doped buffer layer into the bulk region of a Gate Injection Transistor Koushik Bharadwaj, Ashok Ray, Sushanta Bordoloi, Pratima Agarwal and Prof. Gaurav Trivedi		
Design and analysis of a minimally invasive and ECG controlled Ventricular Assistive Device Prajwal Sharma, Prashanthi K, Vinay Chandrashekar, Krishna Nagaraja, Vikas Vazhiyal and Madhav Rao		
A simple Synthesis Process for Combinational QCA Circuits: QSynthesizer Vaishali Dhare and Usha Mehta		
Mapping of Boolean Logic Functions onto 3D Memristor Crossbar Naveen Murali G., P. Satya Vardhan, F Lalchhandama, Kamalika Datta and Indranil Sengupta		
Stability Analysis of SRAM designed using In$_{0.53}$Ga$_{0.47}$As nFinFET with underlap region JAY PATHAK and Anand Darji		
Neuromorphic Circuits on FDSOI Technology for Computer Vision Applications Dinesh Rajasekharan, Amit Ranjan Trivedi and Yogesh Chauhan		
Reconfigurable Digital Logic Gate based on Neuromorphic Approach		

Navin Singhal, M Santosh and S.C. Bose
Realizing Boolean functions using Probabilistic Spin Logic (PSL) Vaibhav Agarwal and Sneh Saurabh
Comparative Study of Analog Matching Structures in 28FDSOI VARUN KUMAR DWIVEDI, Meenakshi Didharia, Madhvi Sharma and Manoj Kumar Sharma
A Model of Spurs for ΔΣ Fractional PLLs Debdut Biswas and Tarun Kanti Bhattacharyya
Exploiting Negative Control Lines and Nearest neighbor for Improved Comparator Design Tathagato Bose, Kamalika Datta and Indranil Sengupta
Intelligent Scheduling of Smart Appliances in Energy Efficient Buildings: A Practical Approach Nilotpal Chakraborty, Arijit Mondal and Samrat Mondal
Design and Implementation of Threshold Logic Functions using Memristors Yaswanth Krishna Yadav Danaboina, Pravanjan Samanta, Kamalika Datta, Indrajit Chakrabarti and Indranil Sengupta
A Transimpedance Amplifier with Improved PSRR at High Frequencies for EMI Robustness Sana Mujeeb and Krishna Kanth Gowri Avalur
On chip RF to DC power converter for biomedical applications Harshal Chapade and Rajesh Zele
Energy Efficient Communication with Lossless Data Encoding for Swarm Robot Coordination Karthik Narayanan, Vinayak Honkote, Dibyendu Ghosh and Swamy Baldev
Multi-Application based Network-on-Chip Design for Mesh-of-Tree topology using Global Mapping and Reconfigurable Architecture Monil Shah, Mohit Upadhyay, Veda Bhanu and Soumya J
Extending STL basic operators used in 3GPP codecs to leverage features of modern DSP architectures Ajay Homkar, Satish Patil, Lukman Rahumathulla, Raj Pawate and Sachin Ghanekar
A Machine Learning Based Approach to Predict Power Efficiency of S-boxes Rajat Sadhukhan, Nilanjan Datta and Debdeep Mukhopadhyay
RF and RFID based Object Identification and Navigation system for the Visually Impaired Gaurav Mishra, Urvi Ahluwalia, Karan Praharaj and Shreyangi Prasad
Design and Implementation of Low-power High-throughput PRNGs for Security Applications Bikram Paul, Apratim Khobragade, Javvaji Soumith, Sushree Sila P. Goswami, Sunil Dutt and Gaurav Trivedi
Hardware Trojan Detection by Stimulating Transitions in Rare Nets Tapobrata Dhar, Surajit Kumar Roy and Chandan Giri
An Enhanced Artificial Bee Colony Algorithm and Automatic Analog CMOS Circuit Design Subhash Patel and Rajesh Thakker
Continuous Transparent Mobile Device Touchscreen Soft Keyboard Biometric Authentication Timothy Dee, Ian Richardson and Akhilesh Tyagi
Design of a Charge Sensitive Amplifier for Silicon Particle Detector in BCD 180 nm Process

Hitesh Shrimali, Ashish Joshi, Indu Yadav, Ettore Ruscino, Valentino Liberali and Attilio Andreazza
WCET-Aware Stack Frame Management of Embedded Systems using Scratchpad Memories Yooseong Kim, Mohammad Khayatian and Aviral Shrivastava
Self-Organizing Maps-based Flexible and High-Speed Packet Classification in Software Defined Networking Shih-Chang Hung, Nick Iliev, Balajee Vamanan and Amit Ranjan Trivedi
A 0.8V VMIN Ultra-Low Leakage High Density 6T SRAM in 40nm CMOS Technology using Repeated-Pulse Wordline Suppression Scheme Ashish Kumar, Mohammad Aftab Alam and Gangaikondam Visweswaran
Tea and Wrap Up