VLSID PhD Forum 2019

Schedule		Title of the Thesis	Author(s)
7th Jan 19 Afternoon	Thesis #1	Machine Learned Machines: Reinforcement Learning Exploration for Architecture Co-optimization	Rahul Jain
	Thesis #2	Energy-Efficient and Secure Network-on-Chip Architectures for DSP Applications	N. Prasad, Indrajit Chakrabarti, and Santanu Chattopadhyay
8th Jan 19 Afternoon	Thesis #3	Assertion Based Analysis of Mixed-Signal Systems	Antara Ain
	Thesis #4	Quantum transport modeling for performance estimation of 2D material based transistors	Madhuchchanda Brahma

Schedule		Title of the Poster	Author(s)
9th Jan 19 Morning	Poster #1	Adaptive Bus-Encoding (ABE) for Transition Reduction on Off-chip and On-chip Buses	Sumantra Sarkar, Anindya Sundar Dhar, and Rahul Rao
	Poster #2	Energy efficient computing and its implications	Patanjali SLPSK
	Poster #3	Online Monitoring based Design-for-Trust Technique to Build a Trusted Hardware Design	Sree Ranjani Rajendran and Nirmala Devi M
	Poster #4	Influence of Body-Bias and Gate-Source Overlap Length on the Analog Performance of Epitaxial Layer Enabled Area Scaled Tunneling FETs	Abhishek Acharya and Anand Bulusu
	Poster #5	Multi-rate Strategies for Power and Bandwidth Optimization in Embedded Control	Rajorshee Raha, Pallab Dasgupta, and Partha Pratim Chakrabarti
9th Jan 19 Afternoon	Poster #6	Error-Tolerant Sample Preparation with Digital Microfluidic Lab-on-Chip	Sudip Poddar, Hafizur Rahaman and Bhargab B. Bhattacharya
	Poster #7	Demonstration of Novel Structures for Improvement in Performance of Tunnel FETs	Navjeet Bagga and Sudeb Dasgupta
	Poster #8	A 125 klx In-Pixel Background Light Subtraction and 144 fps Frame-Rate CMOS Image Sensor for Time-of-Flight 3D Cameras	Chandani Anand and Mukul Sarkar
	Poster #9	Case Study in FPGA Based Hardware-in-the-loop Simulation of Power Electronic Systems	Mini Namboothiripad, Yash Didhe, Mandar Datar, Vinay B.Y. Kumar, Mukul Chandorkar, and Sachin Patkar